FORM PTO-1390 (Modified) (REV 11-98) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER	
010452	
U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR 1.5)	
09/787661	

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/DE99/03069	20 September 1999	21 September 1998

TITLE OF INVENTION

Method of Fabricating an Amorphous or Polycrystalline Layer on an Insulating Region

APPLICANT(S) FOR DO/EO/US

Tillach et al.

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ A copy of the International Search Report (PCT/ISA/210).
8. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.
9. ☒ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
10. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
11. ☒ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 13 to 20 below concern document(s) or information included:

13. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☒ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☒ Certificate of Mailing by Express Mail
20. ☒ Other items or information:

a.) a Notification of the Recording of a Change (Form PCT/IB/306);
b.) a Post Card Receipt

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/787661	PCT/DE99/03069	010452

21. The following fees are submitted:.

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

		CALCULATIONS PTO USE ONLY
☐	Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2) paid to USPTO and International Search Report not prepared by the EPO or JPO **$1,000.00**	
☒	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **$860.00**	
☐	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$710.00**	
☐	International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$690.00**	
☐	International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4) **$100.00**	
	ENTER APPROPRIATE BASIC FEE AMOUNT =	**$860.00**
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).		**$0.00**

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	
Total claims	3 - 20 =	0	x $18.00	**$0.00**
Independent claims	1 - 3 =	0	x $80.00	**$0.00**
Multiple Dependent Claims **(check if applicable)**.			☐	**$0.00**
	TOTAL OF ABOVE CALCULATIONS =			**$860.00**
Reduction of 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 CFR 1.9, 1.27, 1.28) **(check if applicable)**.			☒	**$430.00**
	SUBTOTAL =			**$430.00**
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)).			+	**$0.00**
	TOTAL NATIONAL FEE =			**$430.00**
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) **(check if applicable).**			☐	**$0.00**
	TOTAL FEES ENCLOSED =			**$430.00**
			Amount to be: refunded	$
			charged	$

☒ A check in the amount of **$430.00** to cover the above fees is enclosed.

☐ Please charge my Deposit Account No. in the amount of to cover the above fees.
A duplicate copy of this sheet is enclosed.

☐ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Law Offices of Karl Hormann
86 Sparks Street
Cambridge MA 02138-2216

Tel.: (617)-491-8867

SIGNATURE

Karl Hormann
NAME

26,470
REGISTRATION NUMBER

20 March 2001
DATE

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS (37 CFR 1.9(f) AND 1.27 (c)) - SMALL BUSINESS CONCERN	Docket No. 010452

Serial No.	Filing Date	Patent No.	Issue Date

Applicant/ entee: **Tillack et al.**

Invention: **Method of Fabricating an Amorphous or Polycrystalline Layer on an Insulating Region**

I hereby declare that I am:

- ☐ the owner of the small business concern identified below:
- ☒ an official of the small business concern empowered to act on behalf of the concern identified below:

NAME OF CONCERN: **Institut fuer Halbleiterphysik Frankfurt (Oder) GmbH.**
ADDRESS OF CONCERN: **Walter-Korsing-Strasse 2, D-15230 Frankfurt / Oder, Germany**

I hereby declare that the above-identified small business concern qualifies as a small business concern as defined in 13 CFR 121.3-18, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees under Section 41(a) and (b) of Title 35, United States Code, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the above identified invention described in:

- ☐ the specification filed herewith with title as listed above.
- ☐ the application identified above.
- ☐ the patent identified above.

If the rights held by the above-identified small business concern are not exclusive, each individual, concern or organization having rights to the invention is listed on the next page and no rights to the invention are held by any person, other than the inventor, who could not qualify as an independent inventor under 37 CFR 1.9(c) or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

Each person, concern or organization to which I have assigned, granted, conveyed, or licensed or am under an obligation under contract or law to assign, grant, convey, or license any rights in the invention is listed below:

☒ no such person, concern or organization exists.
☐ each such person, concern or organization is listed below.

FULL NAME _____
ADDRESS _____
☐ Individual ☐ Small Business Concern ☐ Nonprofit Organization

FULL NAME _____
ADDRESS _____
☐ Individual ☐ Small Business Concern ☐ Nonprofit Organization

FULL NAME _____
ADDRESS _____
☐ Individual ☐ Small Business Concern ☐ Nonprofit Organization

FULL NAME _____
ADDRESS _____
☐ Individual ☐ Small Business Concern ☐ Nonprofit Organization

Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

NAME OF PERSON SIGNING: _____
TITLE OF PERSON SIGNING
OTHER THAN OWNER: _____
ADDRESS OF PERSON SIGNING: Im Technologiepark 25
D-15236 Frankfurt (Oder)
Germany

SIGNATURE: _____ _____ DATE: March 14, 2001

Prof.A.Ourmazd F.Weinl
Scientific Director Adm.Director

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

International Application No.: PCT/DE99/03069
International Filing Date: 20 September 1999
By: Tillach et al.
For: Method of Fabricating an Amorphous or Polycrystalline Layer on an Insulating Region

86 Sparks Street
Cambridge MA 02138-2216
20 March 2001

Hon.
Assistant Commissioner for Patents
Washington DC 20231

Box PCT

Preliminary Amendment Based on Specification and Claims as Amended Pursuant to Atricle 19 and/or 34 (2)(b) of the Patent Cooperation Treaty

Sir:

With a view to avoiding claims surcharge fees otherwise due and to placing their application in a condition believed to comply with current U.S. patent prosecution standards, Applicants courteously request that their instant application be amended as follows.

In the Specification:

Page 1, line 7: insert --BACKGROUND OF THE INVENTION.

1. Field of the Invention.--;

page 2, line 2: insert --2. The Prior Art.--;

line 12: insert --OBJECT OF THE INVENTION.--;

line 20: insert --BRIEF SUMMARY OF THE INVENTION.--;

page 3, line 2: insert --DESCRIPTION OF THE SEVERAL DRAWINGS.--;

line 15: insert --DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS.--;

page 8, line 1: cancel "Patent Claims" and substitute therefor --What is claimed is:--; and

page 9, line 1: cancel "Abstract" and substitute therefor --ABSTRACT OF THE DISCLOSURE.--.

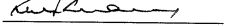
In the claims:

Claim 1, line 1: change "Method" to --A method--;

claim 2, line 1: change "Method" to --The method--; and

claim 3, line 1: change "Method" to --The method-- and cancel "or 2".

Respectfully submitted,



Karl Hormann
Registration No.: 26,470

Area Code (617)-491-8867

Method of Fabricating an Amorphous or Polycrystalline Layer on an Insulating Region.

The invention relates to a method of fabricating an amorphous or polycrystalline layer on an insulating region.

In semiconductor technology amorphous or polycrystalline layers are applied in vastly different fields.

An important field of application of such layers is vertical bipolar transistors for high speed applications which, after mono-poly-silicon technology, may be fabricated with epitaxially incorporated base layers. Owing to the poor seeding of the conventional SiO_2-layer used as an insulating layer, the amorphous or polycrystalline silicon layer is usually thinner than an epitaxially grown layer. Furthermore, homogeneous precipitation is made difficult by the poor and irregular seeding of the SiO_2-layer. In the case of polycrystalline silicon, grains of different size are formed which leads to a rough surface and irregular electrical properties. The problems increase drastically if instead of Si, SiGe or SiGe:C is being used. In such cases, when precipitating the epitaxial layer seeding is so bad that no polycrystalline or amorphous precipitation on the SiO_2 is possible within the time usually required for the precipitation of the epitaxial layer.

As regards the thickness of the epitaxial layer, there are two different requirements. Within the region of the emitter the thickness of the layer between the highly doped emitter and the base should be sufficiently thin. In the area of the outer base, a greater thickness is advantageous to provide for

low resistance of the base connector.

PATENT ABSTRACTS OF JAPAN, Vol. 012, No. 207 (E-621), 14 June 1988 (1988-06-14) & JP 63006874 A (FUJITSU LTD), 12 January 1988 (1988-01-12) and PATENT ABSTRACTS OF JAPAN, Vol. 011, No. 217 (E-523), 14 July 1987 (1987-07-14) & JP 62036865 A (FUJITSU LTD), 17 February 1987 (1988-01-12) in particular, disclose semiconductor components which contain a substrate, an SiO_2 layer, an Si_3Ni_4 layer on the SiO_2 layer, a polycrystalline silicon layer on the Si_3Ni_4 layer and a epitaxial silicon layer applied on the substrate simultaneously with the polycrystalline silicon layer.

It is an object of the invention to propose a method of fabricating an amorphous or polycrystalline layer on an insulating region by which in contrast to methods hitherto used the thickness of the amorphous or polycrystalline layer is greater, the homogeneity of the precipitation is improved and the roughness of the surface is thus reduced. At the same time, the insulating properties of the insulating region are at least to be maintained.

In accordance with the invention, the object is being satisfied by improving the seeding during precipitation of the amorphous or polycrystalline layer by applying a suitable seeding layer of good seeding capacity and insulating properties on the insulating region. As a result the thickness of the amorphous or polycrystalline layer is significantly greater than it would be in the absence of a seeding layer. The greater thickness of the amorphous or polycrystalline layer is obtained by improved seeding which leads to shortening of the induction period (idle time) for the precipitation on the insulating layer. The better and more uniform seeding of the seeding layer leads to a homogenous precipitation. This leads to uniform electrical properties. Using a SiO_2-layer as an insulating layer and a silicon nitride layer

as a seeding layer is particularly suitable.

Aside from the claims the characteristics of the invention will be apparent from the specification and the drawings, whereby individual characteristics by themselves or as subcombination are deemed to be protectable embodiments for which protection is hereby claimed. Embodiments of the invention are depicted in the drawings and will be described in greater detail hereinafter. In the drawings:

Fig. 1 is a schematic presentation of a bipolar transistor;
Fig. 2 is a schematic presentation of a bipolar transistor according to Fig. 1 during its fabrication;
Fig. 3 is a schematic presentation of a layer structure before epitaxy; and
Fig. 4 is a schematic presentation of a layer structure following epitaxy.

Example 1:

The invention will now be described in connection with a mono-poly-silicon process.

Fig. 1 schematically depicts a bipolar transistor 10. A collector region of conductivity type II has been fabricated on a semiconductor substrate region 11 of conductivity type I. If emitter and collector are, for instance, n-conductive, the base is type p, and *vice versa*. Several processes are known which provide for suitable collector doping. Among these is, for instance, the structure shown in Fig. 1 with a highly doped buried layer 12 and a less doped epitaxial layer 13 as well as implanted retrograde well. In the example here shown, field insulating region 14 separates the bipolar transistor from other components not shown in the drawing and the collector connection region from the active region of the transistor. Other suitable insulating techniques are also known, such as, for instance, spaced mesa arrangements. In this example, a buried implant 20 has been incorporated to

reduce the resistance between the highly doped contact layer 21 made of poly-silicon and the buried layer 12. In accordance with the invention, a layer 28 of excellent seeding capacity and insulating properties (seeding layer) is present on the insulating region. In the present embodiment, silicon nitride is used for this purpose.

An epitaxial layer sequence consisting of a buffer layer 15, an *in situ* doped base layer 16 of conductivity type I as well as a cover layer 17, is covering the emitter region in the active transistor region and at least a section of the insulating region provided with the seeding layer 28. The epitaxial layer structured outside of the active transistor region is covered by a non-conductive material 18.

The use of a thick polycrystalline layer on the insulating region is to be considered as essential in the context of the invention. The specific values of the thickness, the dopant content as well as the material composition of the base are to be set in accordance with the requirements of the function of the bipolar transistor and, in accordance with the invention, they are not subject to any special requirements. In the example shown, the base layer consists of silicon, is p-doped with $2 \cdot 10^{18}$ cm^{-3} and is assumed to have a thickness of 40 nm. However, other material compositions and doping profiles may be used as well. It is possible t use a thin cover layer 17 over the base layer. Doping of the emitter in the mono-silicon is ensured by outdiffusion of dopant 22 from the highly doped poly-silicon contact layer 21. The precipitated thickness of the cover layer 17 typically is 50 nm.

Whilst the buffer, basis and cover layer grow monocrystalline over the silicon substrate, polycrystalline layers 19 are formed over the insulating region 14 provided with the seeding layer 28. In accordance with the invention, the thickness of the precipitated polycrystalline layer is increased by the use of the seeding layer 28. Outside of the poly-silicon contact layer

21 overlapping the active transistor region doping in the base connection region has been additionally increased by implantation 23. The insulating layer 24 separates emitter, base and collector contact. The transistor structure is completed by the metal contacts for emitter 25, base 26 and collector 27.

The fabrication of a bipolar transistor in accordance with the invention with be described hereafter. The method in accordance with the invention proceeds on the basis of the structure shown in Fig. 2. Following photolithographic structuring, a highly doped n-layer 12 is incorporated by implantation in the p-doped silicon substrate 11, and annealed. Thereafter, a weakly doped n-layer 13 is precipitated epitaxially. The active region is defined by conventional process steps and generate insulating regions 14 (e.g. LOCOS) in the remaining regions. In accordance with the invention, a seeding layer 28 is precipitated over the whole surface and is opened over the active transistor region. Preferably, silicon nitride is used for the seeding layer 28. The buffer layer 15, the base layer 16 and the cover layer 17 are precipitated by means of differential epitaxy. By the use of the seeding layer 28 seeding of the insulating region is improved. In this manner the idle time for the precipitation on the insulating region is reduced. As a result the polycrystalline layer 19 on the insulator is substantially thicker than by precipitation without using the seeding layer 28.

After photolithographically structuring a mask the precipitated silicon or poly-silicon layers outside of the later transistor and base connection region on the insulating region 14 are removed by a plasma etching step and an etching stop. Thereafter, a non-conductive material 18, preferably oxide, is applied.

By photolithographically structuring a lacquer mask the collector connection region will now be exposed and the buried implant 20 will be

applied. After the lacquer mask has been removed and after structuring of a further lacquer mask, the oxide layer 18 is wet chemically etched in the collector connection region as well as in the emitter region. The process is continued by precipitation of an amorphous silicon layer. This may be doped by implantation *in situ*, during or following the precipitation. Emitter and collector contact regions are masked by a lithographic step. In the remaining regions, the amorphous silicon is removed by a plasma etching step with a stop on the SiO_2 layer. During the ensuing implantation of the base connection regions the emitter and collector contact regions are protected by the present masking. Tempering will take place after removal of the mask and covering of the generated surface with oxide for annealing the implantation defects and for forming the poly-emitter. The process is completed by opening the via holes for emitter, base and collector and by a standard metallization of the transistor contacts.

Example 2:

The basis for the method in accordance with the invention in this embodiment is the layer structure before epitaxy shown in Fig. 2. An insulating layer 31 consisting of SiO_2 has been precipitated on silicon substrate 30 and has been structured by means of photolithographic processes. In accordance with the invention the insulating layer 31 is additionally partially covered by a structured seeding layer 32 consisting of silicon nitride. As shown in Fig. 4, the result of the epitaxy step is the generation of a mono-crystalline layer on uncovered silicon substrate. The polycrystalline layers 33 grown on the insulating layer 31 and seeding layer 32 are different in structure and thickness. Compared to the polycrystalline layer 33 on the insulating layer 31 the polycrystalline layer 33 on the seeding layer 32 is of a more homogenous and more finely grained structure of greater thickness.

On the basis of concrete embodiments there has been described, in

the context of the present invention, a method for fabricating an amorphous or polycrystalline layer on an insulating region. It is, however, to be mentioned that the present invention is not limited to the details of the embodiments of the specification since changes and alterations are being claimed within the scope of the claims.

Patent Claims

1. Method of fabricating an amorphous or polycrystalline silicon layer consisting, in particular of silicon or sailicon germanium, on an insulating region (14, 31), whereby the amorphous or polycrystalline layer (19, 33) may contain, in particular, carbon or oxygen as a diffusion inhibiting agent, **characterized by the fact that** for improving seeding a seed initiation layer (28, 32) of good seeding capacity and insulating properties is fabricated on the insulating region (14, 31) because of which during precipitation of amorphous or polycrystalline layers (19, 33) the thickness is substantially greater, the homogeneity of the precipitation is improved, the distribution of grain size in polycrystalline layers (19, 33) is more uniform and surface roughness is less than if the seeding layer (28, 32) is omitted.

2. Method of claim 1, **characterized by the fact that** an SiO_2-layer is preferably used as insulating layer (14, 31) and silicon nitride is preferably used as seeding layer (28, 32).

3. Method of claim 1 or 2, **characterized by the fact that** the seeding layer (28, 32) is applied before a differential epitaxy and thus the amorphous or polycrystalline layer (19, 33) is formed on the insulating region (14, 31) and an epitaxial layer is formed on the monocrystalline substrate (11, 30).

Abstract

The invention aims at providing a method of fabricating an amorphous or polycrystalline layer on an insulating region which compared to known methods increases the thickness of the amorphous or polycrystalline layer and improves the homogeneity of the precipitation thus resulting in lower surface roughness while at least maintaining the insulating properties of the insulating region. To this end a suitable seeding layer (28, 29), preferably of silicon nitride, is deposited so that the seeding capacity and insulating properties of the SiO_2 insulating region (14, 31) during precipitation of the amorphous or polycrystalline Si or SiGe lkayers (15, 16, 17, 33) are improved.

Docket No.
010452

Declaration and Power of Attorney For Patent Application

English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Method of Fabricating an Amorphous or Polycrystalline Layer on an Insulating Region

the specification of which

(check one)

☒ is attached hereto.

☐ was filed on _____ as United States Application No. or PCT International Application Number _____

and was amended on _____

(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Not Claimed
198 45 792.8	Germany	21 September 1998	☐
(Number)	(Country)	(Day/Month/Year Filed)	
			☐
(Number)	(Country)	(Day/Month/Year Filed)	
			☐
(Number)	(Country)	(Day/Month/Year Filed)	

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below:

N/A	
(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)

I hereby claim the benefit under 35 U. S. C. Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, C. F. R., Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

PCT/DE99/03069	20 September 1999	Pending
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

Karl Hormann, Esq., Registration No. 26,470 (1)

Send Correspondence to: **Law Offices of Karl Hormann**
86 Sparks Street
Cambridge MA 02138-2216

Direct Telephone Calls to: *(name and telephone number)*
Mr Hormann @ 617.491.8867

(1.00)

Full name of sole or first inventor
Bernd Tillack

Sole or first inventor's signature
Bernd Tillack

Date
Mard 13 01
13 March 2001

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Post Office Address
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Full name of second inventor, if any
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Second inventor's signature
Bernd Heinemann

Date
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13 March 2001

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Citizenship
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300

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Third inventor's signature
X Dieter Knoll

Date
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13 March 2001

Citizenship
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same as residence

400

Full name of fourth inventor, if any
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Fourth inventor's signature
X Karl-Ernst Ehwald

Date
13.3.01

Residence
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13 March 2001

Citizenship
German

Post Office Address
same as residence

500

Full name of fifth inventor, if any
Dirk Wolansky Dirk Wolansky

Fifth inventor's signature
X Dirk Wolansky

Date
03/13/01

Residence
Lennestrasse 4, D-15234 Frankfurt / Oder, Germany DEX

13 March 2001

Citizenship
German

Post Office Address
same as residence

Full name of sixth inventor, if any
n/a

Sixth inventor's signature

Date

Residence

Citizenship

Post Office Address